UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,582	08/05/2003	Takayuki Tamura	XA-9908	7087

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
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EXAMINER
DARE, RYAN A

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 11/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/633,582	TAMURA ET AL.
	Examiner	Art Unit	
	Ryan Dare	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>08/05/2003</u>.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-17</u> is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) <u>1-17</u> is/are rejected.
7) ☒ Claim(s) <u>1, 7, 14, and 17</u> is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on <u>08/05/2003</u> is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a) ☒ All   b) ☐ Some * c) ☐ None of:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>08/05/2003</u>.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____ .

DETAILED ACTION

Drawings

1.   The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5)

because they include the following reference character(s) not mentioned in the

description: S65 in fig. 15. Corrected drawing sheets in compliance with 37 CFR

1.121(d), or amendment to the specification to add the reference character(s) in the

description in compliance with 37 CFR 1.121(b) are required in reply to the Office action

to avoid abandonment of the application. Any amended replacement drawing sheet

should include all of the figures appearing on the immediate prior version of the sheet,

even if only one figure is being amended. Each drawing sheet submitted after the filing

date of an application must be labeled in the top margin as either "Replacement Sheet"

or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the

examiner, the applicant will be notified and informed of any required corrective action in

the next Office action. The objection to the drawings will not be held in abeyance.

2.   The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4)

because reference characters "S33" and "S24" have both been used to designate the

"writing from host finished" decision block in fig. 11. Corrected drawing sheets in

compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid

abandonment of the application. Any amended replacement drawing sheet should

include all of the figures appearing on the immediate prior version of the sheet, even if

only one figure is being amended. Each drawing sheet submitted after the filing date of

an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next

Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3.   Claims 1, 7, 14 and 17 are objected to because of the following informalities:

They use language such as "capable of" and "can perform" which only indicate the

absence of anything preventing the memory from performing a specific function or

having a specific property, and do not necessarily indicate that the claimed invention

possesses those properties. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4.   Claim 1 recites the limitation "said nonvolatile memory cell" in lines 7 and 10.

There is insufficient antecedent basis for this limitation in the claim. It is unclear

whether the invention is directed to one specific nonvolatile memory cell out of the

plurality of cells claimed in lines 3-4, or whether each cell in the plurality possesses the

claimed properties.

5.   Claim 14 recites the limitation "said nonvolatile memory cell" in lines 8 and 11.

There is insufficient antecedent basis for this limitation in the claim. It is unclear

whether the invention is directed to one specific nonvolatile memory cell out of the

plurality of cells claimed in lines 3-4, or whether each cell in the plurality possesses the

claimed properties.

Claim Rejections - 35 USC § 102

6.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by
> another filed in the United States before the invention by the applicant for patent or (2) a patent
> granted on an application for patent by another filed in the United States before the invention by the
> applicant for patent, except that an international application filed under the treaty defined in section
> 351(a) shall have the effects for purposes of this subsection of an application filed in the United States
> only if the international application designated the United States and was published under Article 21(2)
> of such treaty in the English language.

7.   Claims 1, 5-6 and 14-16 are rejected under 35 U.S.C. 102(e) as being

anticipated by Chang, US Patent 6,529,405.

8.   With respect to claim 1, Chang teaches a nonvolatile memory apparatus

comprising a nonvolatile memory and a controller, in fig. 3, where numeral 100 is the

controller and flash memory array 40 is the nonvolatile memory,

wherein said nonvolatile memory has a plurality of nonvolatile memory cells each

capable of storing information of n bits (n: integer of 2 or larger), and can perform a first

reading operation of outputting information read from said nonvolatile memory cell as

information of m bits (m: integer smaller than n) and a second reading operation of

outputting information read from said nonvolatile memory cell as information of n bits, in

col. 5, lines 36-50, and

wherein said controller performs the first reading operation to read first

information from said nonvolatile memory and performs the second reading operation to

read second information from said nonvolatile memory, in col. 5, lines 36-50.

9.   With respect to claim 5, Chang teaches the nonvolatile memory apparatus

according to claim 1,

wherein said nonvolatile memory cell has a threshold voltage included in one of

four or more threshold voltage distributions according to information to be stored, in fig.

1B and col. 2, lines 30-39, and

wherein at the time of storing said first information into said nonvolatile memory

cell, said nonvolatile memory uses a predetermined voltage between said threshold

voltage distributions as a boundary, sets, as the threshold voltage of the nonvolatile

memory, any of threshold voltage distributions of voltages higher than said

predetermined voltage or threshold voltage distributions of voltages lower than said

predetermined voltage, and compares said predetermined voltage with the threshold

voltage of a nonvolatile memory cell in said first reading operation, thereby reading m-

bit information, in fig. 1B and col. 2, lines 30-39.

10.   With respect to claim 6, Chang teaches the nonvolatile memory apparatus

according to claim 5, wherein the threshold voltage of a nonvolatile memory cell in

which said first information is stored is a voltage selected from a voltage in an upper-

limit threshold voltage distribution and a voltage in a lower limit threshold voltage

distribution, in fig. 1B and col. 2, lines 30-39.

11.   With respect to claim 14, Chang teaches a nonvolatile memory apparatus

comprising a nonvolatile memory and a controller,

wherein said nonvolatile memory has a plurality of nonvolatile memory cells each

of which can be set in an information storing state included in one of four or more

information storing states, and can perform a first reading operation of outputting

information read from said nonvolatile memory cell which is set in said information

storing state as information of m bits (m: integer of 1 or larger) and a second reading

operation of outputting information read from said nonvolatile memory cell which is set

in said information storing state as information of n bits (n: integer larger than m), in col.

5, lines 36-50, and

wherein said controller performs the first reading operation to read first

information from said nonvolatile memory and performs the second reading operation to

read second information from said nonvolatile memory, in col. 5, lines 36-50.

12.   With respect to claim 15, Chang teaches the nonvolatile memory apparatus

according to claim 14, wherein an information storing state included in one of said four

or more information storing states is a threshold voltage state included in one of four or

more threshold voltage distributions of a nonvolatile memory cell, in fig. 1B and col. 2,

lines 30-39.

13.   With respect to claim 16, Chang teaches the nonvolatile memory apparatus

according to claim 15, wherein at the time of storing said first information into said

nonvolatile memory cell, said nonvolatile memory sets, as a threshold voltage of the

nonvolatile memory cell, a voltage selected from a voltage in said threshold voltage

distribution of the upper limit and a voltage in said threshold voltage distribution of the

lower limit, in fig. 1B and col. 2, lines 30-39.

Claim Rejections - 35 USC § 103

14.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15.   The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

16.   Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Chang as applied to claims 1, 5-6 and 14-16 above, and further in view of Shinohara,

US Patent 5,742,934.

17.   With respect to claim 2, Chang teaches all other limitations of the parent claim as

discusses supra, but fails to teach that the first information is validity management

information. Shinohara et al. teaches the nonvolatile memory apparatus according to

claim 1, wherein said first information is validity management information indicative of

validity of a storage area of said second information, in fig. 2, sector management area 101 and col. 3, lines 65-67.

18.   It would have been obvious to one of ordinary skill in the art, having the teachings of Chang and Shinohara before him at the time the invention was made, to modify the nonvolatile memory apparatus of Chang with the nonvolatile memory apparatus of Shinohara in order to identify defective blocks, as taught by Shinohara et al. in col. 6 lines 41-47.

19.   With respect to claim 3, Chang and Shinohara teach all other limitations of the parent claims as discussed supra, but Chang fails to teach the use of validity management information. Shinohara teaches the nonvolatile memory apparatus according to claim 2, wherein when the nonvolatile memory is operated according to an instruction from the controller, in col. 3, lines 45-47, said controller checks validity of a storage area of said second information on the basis of the validity management information read from the nonvolatile memory by performing the first reading operation and, when it is determined that the storage area is valid, performs the second reading operation to read the second information from the nonvolatile memory, in fig. 7, decision block S35 and block S38, with reference to the specification, lines 26-42.

20.   With respect to claim 4, Chang and Shinohara teach all other limitations of the parent claims as discussed supra, but Chang fails to teach the use of validity management information. Shinohara teaches the nonvolatile memory apparatus according to claim 3, wherein said controller checks validity of a storage area of said second information on the basis of validity management information read from the

nonvolatile memory by performing the first reading operation, when it is determined that the storage area is invalid, checks validity of the storage area of said second information on the basis of validity management information read from the nonvolatile memory by performing the first reading operation on an alternative area of the storage area of said second information and, when the storage area is valid, performs the second reading operation to read the second information from the alternative area, in fig. 7, S35, S35 and S38, with reference to the specification, lines 26-42. The alternative area is the redundant storage area represented by blocks M through M+r in fig. 2.

21.   Claims 7-13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang and Shinohara as applied to claims 1-6 and 14-16 above, and further in view of Norman et al., US Patent 5,974,499.

22.   With respect to claim 7, Chang and Shinohara teach all other limitations of the parent claims as discussed supra, but fail to teach the use of a memory buffer to a nonvolatile memory cell. Norman et al. teach the nonvolatile memory apparatus according to claim 1, wherein said controller can output second information read from the nonvolatile memory by said second reading operation to the outside, and can supply said second information input from the outside to the nonvolatile memory, and wherein said nonvolatile memory has a memory buffer which can temporarily store second information read said second reading operation before the second information is supplied to said controller and can temporarily store second information supplied from

said controller before said second information is stored into said nonvolatile memory

cell, in fig. 4, I/O buffer 52, and described in col. 6, line 48 through col. 7, line 7.

23.   It would have been obvious to one of ordinary skill in the art to modify the

nonvolatile memory apparatus of Chang and Shinohara with the nonvolatile memory

apparatus of Norman et al. in order to control the direction of data (either or into or out

of) the flash memory, as taught by Norman et al. in col. 6, line 65 through col. 7, line 4.

24.   With respect to claim 8, Chang, Shinohara and Norman et al. teach all other

limitations of the parent claims, but Chang and Shinohara fail to teach a memory buffer

and a method of bypassing it. Norman et al. teach the nonvolatile memory apparatus

according to claim 7, wherein said nonvolatile memory outputs first information by

bypassing said memory buffer at the time of reading first information by said first

reading operation, in col. 6, lines 51-54.

25.   It would have been obvious to one of ordinary skill in the art to modify the

nonvolatile memory apparatus of Chang and Shinohara with the nonvolatile memory

apparatus of Norman et al. in order for the memory array to be accessed directly for

testing purposes, as taught by Norman at el. in col. 6, lines 51-54.

26.   With respect to claim 9, Chang, Shinohara and Norman et al. teach all other

limitations of the parent claims and Shinohara et al. teaches the nonvolatile memory

apparatus according to claim 8, wherein said first information is validity management

information indicative of validity of a storage area of said second information, in fig. 2,

sector management area 101 and col. 3, lines 65-67.

27.   It would have been obvious to one of ordinary skill in the art to modify the

nonvolatile memory apparatus of Chang and Shinohara with the nonvolatile memory

apparatus of Norman et al. in order to control the direction of data (either or into or out

of) the flash memory, as taught by Norman et al. in col. 6, line 65 through col. 7, line 4.

28.   With respect to claim 10, Chang, Shinohara and Norman et al. teach all other

limitations of the parent claims and Shinohara teaches the nonvolatile memory

apparatus according to claim 9, wherein when the nonvolatile memory is operated

according to an instruction from the controller, in col. 3, lines 45-47, said controller

checks validity of a storage area of said second information on the basis of the validity

management information read from the nonvolatile memory by performing the first

reading operation and, determines that the storage area is valid, in fig. 7, decision block

S35 and block S38, with reference to the specification, lines 26-42. Shinohara fails to

teach writing information into a buffer and then into a memory cell. Norman et al. teach

writing the data into a memory buffer and then writing it into a memory cell, in col. 7,

lines 17-21.

29.   It would have been obvious to one of ordinary skill in the art to modify the

nonvolatile memory apparatus of Chang and Shinohara with the nonvolatile memory

apparatus of Norman et al. in order to control the direction of data (either or into or out

of) the flash memory, as taught by Norman et al. in col. 6, line 65 through col. 7, line 4.

30.   With respect to claim 11, Chang, Shinohara and Norman et al. teach all other

limitations of the parent claims as discussed supra and Shinohara teaches the

nonvolatile memory apparatus according to claim 10, wherein said controller checks

validity of a storage area of said second information on the basis of validity

management information read from the nonvolatile memory by performing the first

reading operation, when it is determined that the storage area is invalid, checks validity

of the storage area of said second information on the basis of validity management

information read from the nonvolatile memory by performing the first reading operation

on an alternative area of the storage area of said second information and, determines

when the storage area is valid, in fig. 7, S35, S35 and S38, with reference to the

specification, lines 26-42. The alternative area is the redundant storage area

represented by blocks M through M+r in fig. 2. Shinohara fails to teach writing

information into a buffer and then into a memory cell. Norman et al. teach writing the

data into a memory buffer and then writing it into a memory cell, in col. 7, lines 17-21.

31.   It would have been obvious to one of ordinary skill in the art to modify the

nonvolatile memory apparatus of Chang and Shinohara with the nonvolatile memory

apparatus of Norman et al. in order to control the direction of data (either or into or out

of) the flash memory, as taught by Norman et al. in col. 6, line 65 through col. 7, line 4.

32.   With respect to claim 12, Chang, Shinohara and Norman et al. teach all other

limitations of the parent claims as discussed supra, but Chang and Shinohara et al. fail

to teach a controller buffer. Norman et al. teach the nonvolatile memory apparatus

according to claim 7, wherein said controller has a controller buffer for temporarily

holding second information supplied from the outside and temporarily holding second

information read from the nonvolatile memory and supplied, in fig. 33 and col. 32, lines

23-30.

33.   It would have been obvious to one of ordinary skill in the art to modify the

nonvolatile memory apparatus of Chang and Shinohara with the nonvolatile memory

apparatus of Norman et al. in order to control the direction of data (either or into or out

of) the flash memory, as taught by Norman et al. in col. 6, line 65 through col. 7, line 4.

34.   With respect to claim 13, Chang, Shinohara and Norman et al. teach all other

limitations of the parent claims as discussed supra, but Chang and Shinohara et al. fail

to teach a controller buffer. Norman et al. teach the nonvolatile memory apparatus

according to claim 12, wherein said controller supplies data from the controller buffer to

the memory buffer, after that, stores the data in the memory buffer to a nonvolatile

memory cell and, in parallel with the storing operation, can input another data from the

outside into the controller buffer, in col. 32, lines 23-30 which teach putting the data on

the data bus 42. Once that happens, the controller buffer is free to store more data, as

the data from the data bus is stored into I/O buffer 52.

35.   It would have been obvious to one of ordinary skill in the art to modify the

nonvolatile memory apparatus of Chang and Shinohara with the nonvolatile memory

apparatus of Norman et al. in order to control the direction of data (either or into or out

of) the flash memory, as taught by Norman et al. in col. 6, line 65 through col. 7, line 4.

36.   With respect to claim 17, Chang and Shinohara teach all other limitations of the

parent claims as discussed supra but fail to teach a memory buffer. Norman et al. teach

the nonvolatile memory apparatus according to claim 16,

        wherein said nonvolatile memory has a memory buffer which can hold second

information read as n-bit information from each of a plurality of nonvolatile memory cells

by said second reading operation, supply the second information to the controller, hold

second information supplied from said controller, in fig. 4, I/O buffer 52, and described

in col. 6, line 48 through col. 7, line 7.

Chang teaches to set one nonvolatile memory cell every n bits, at a threshold

voltage included in one of four threshold voltage distributions, in fig. 1B and col. 2, lines

30-39.

wherein the first information read as m-bit information from each of the plurality of

nonvolatile memory cells by said first reading operation to said controller, in col. 5, lines

36-50.

Norman et al. teach bypassing the memory buffer in col. 6, lines 51-54.

37.   It would have been obvious to one of ordinary skill in the art to modify the

nonvolatile memory apparatus of Chang and Shinohara with the nonvolatile memory

apparatus of Norman et al. in order to control the direction of data (either or into or out

of) the flash memory, as taught by Norman et al. in col. 6, line 65 through col. 7, line 4.

Conclusion

38.   The prior art made of record on form PTO-892 and not relied upon is considered

pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to

consider these references fully when responding to this action. The documents cited

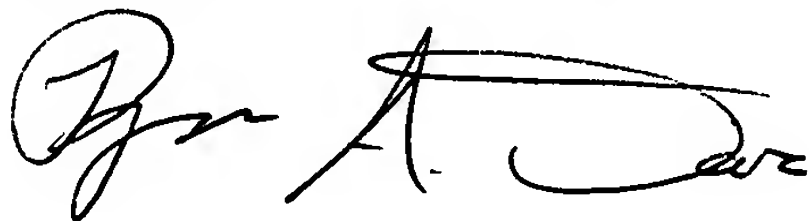therein teach similar nonvolatile memory devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan Dare
November 3, 2005

MATTHEW D. ANDERSON
PRIMARY EXAMINER